

FIG. 1

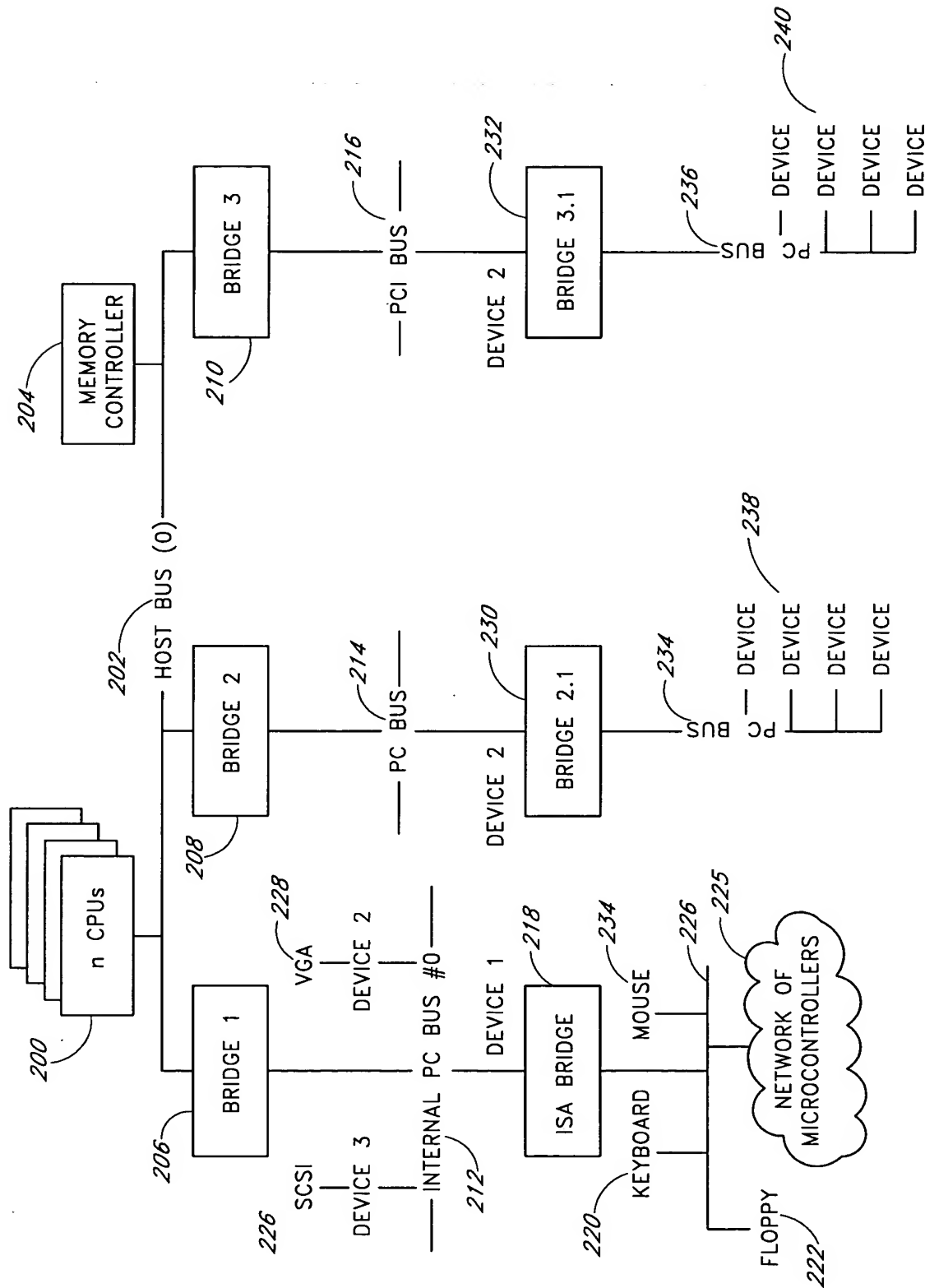


FIG. 2

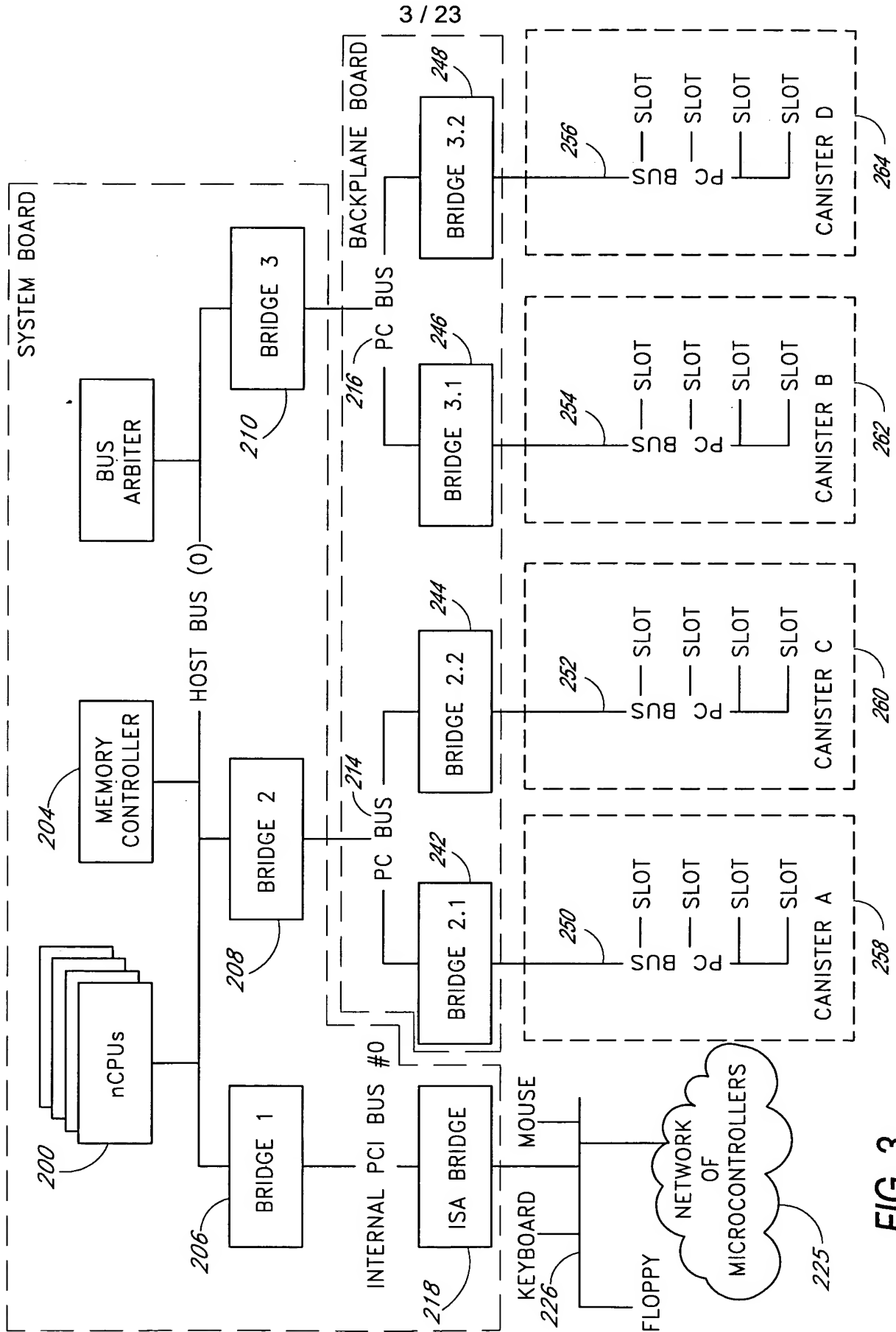


FIG. 3

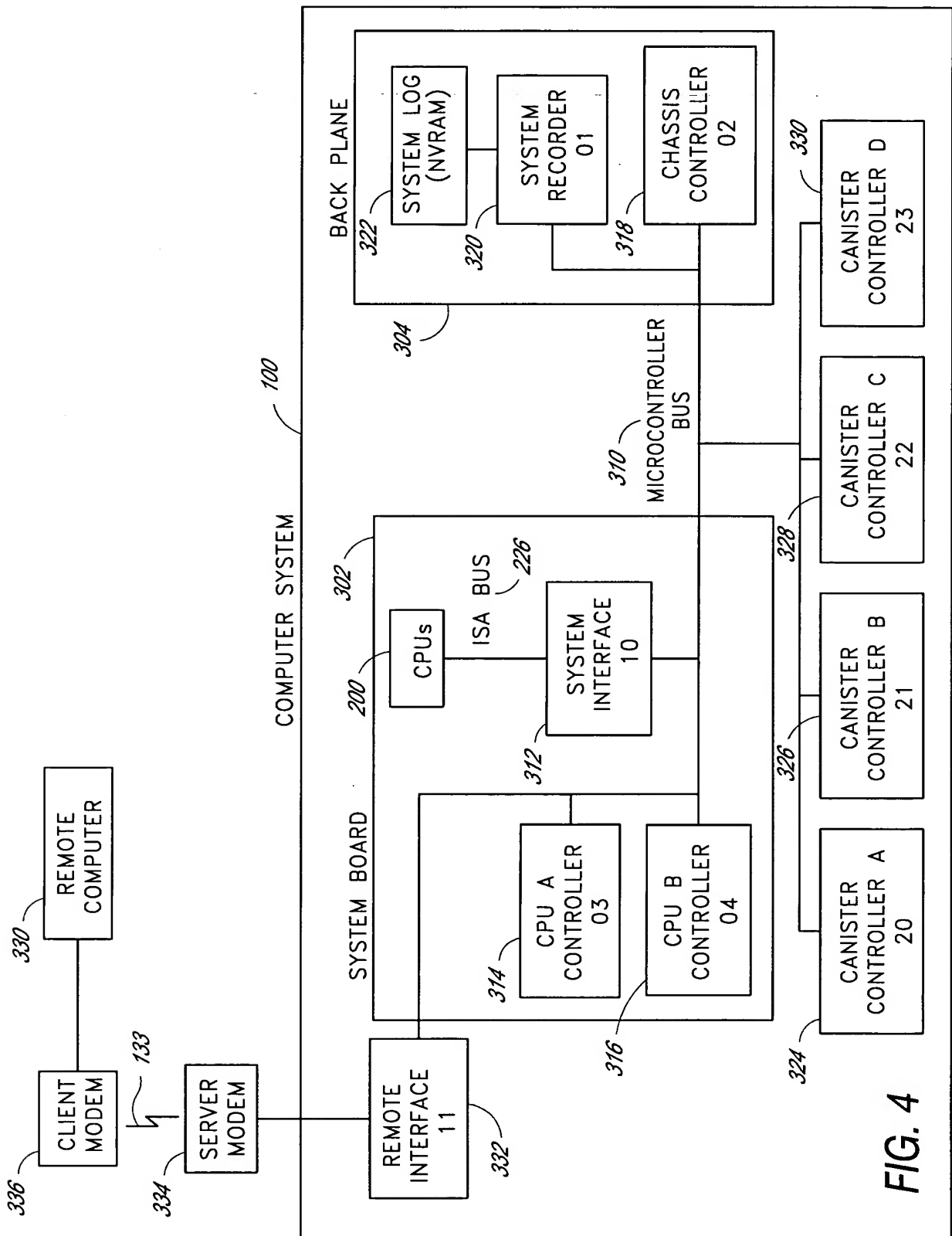


FIG. 4

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Microcontroller Network Bus

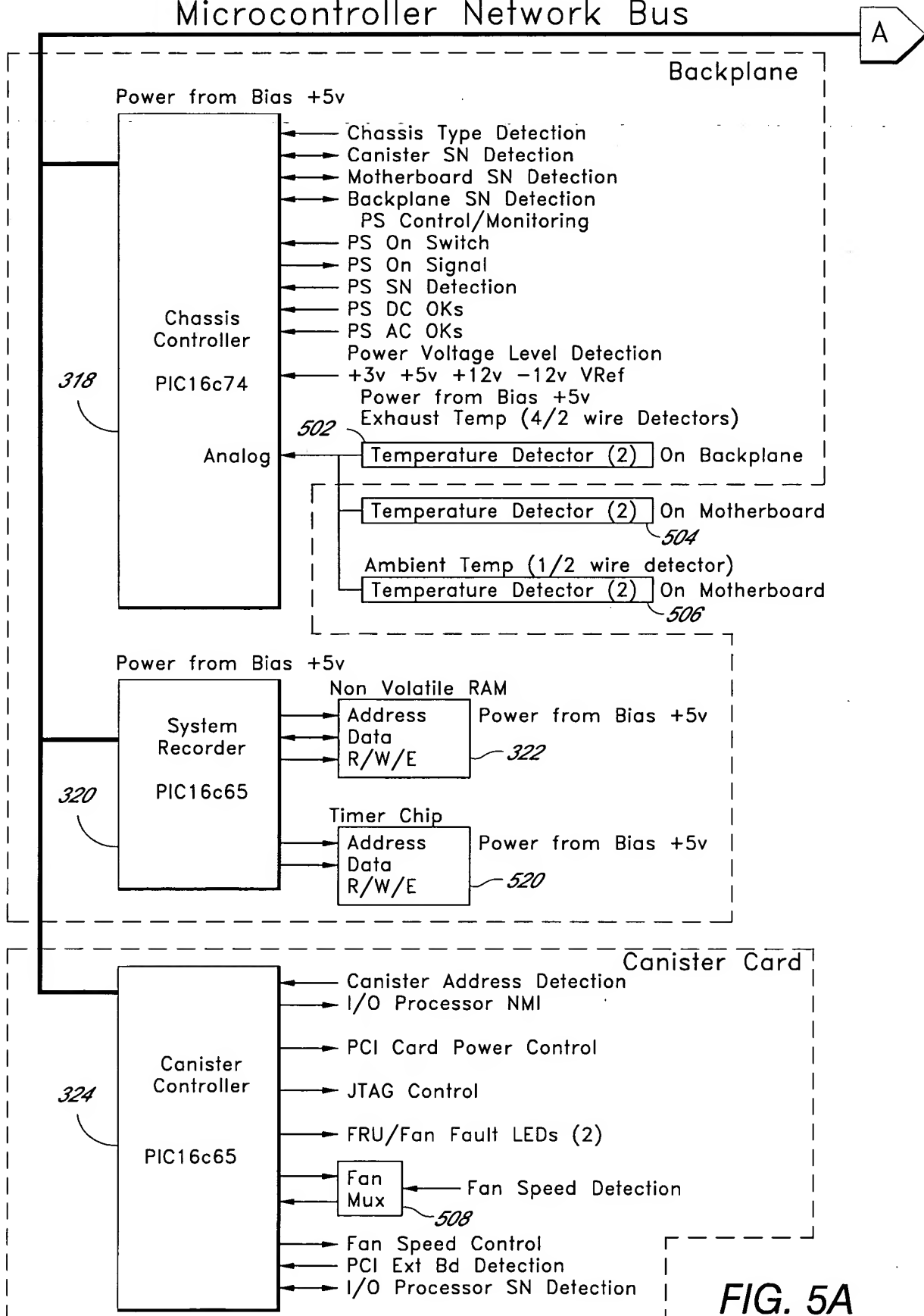
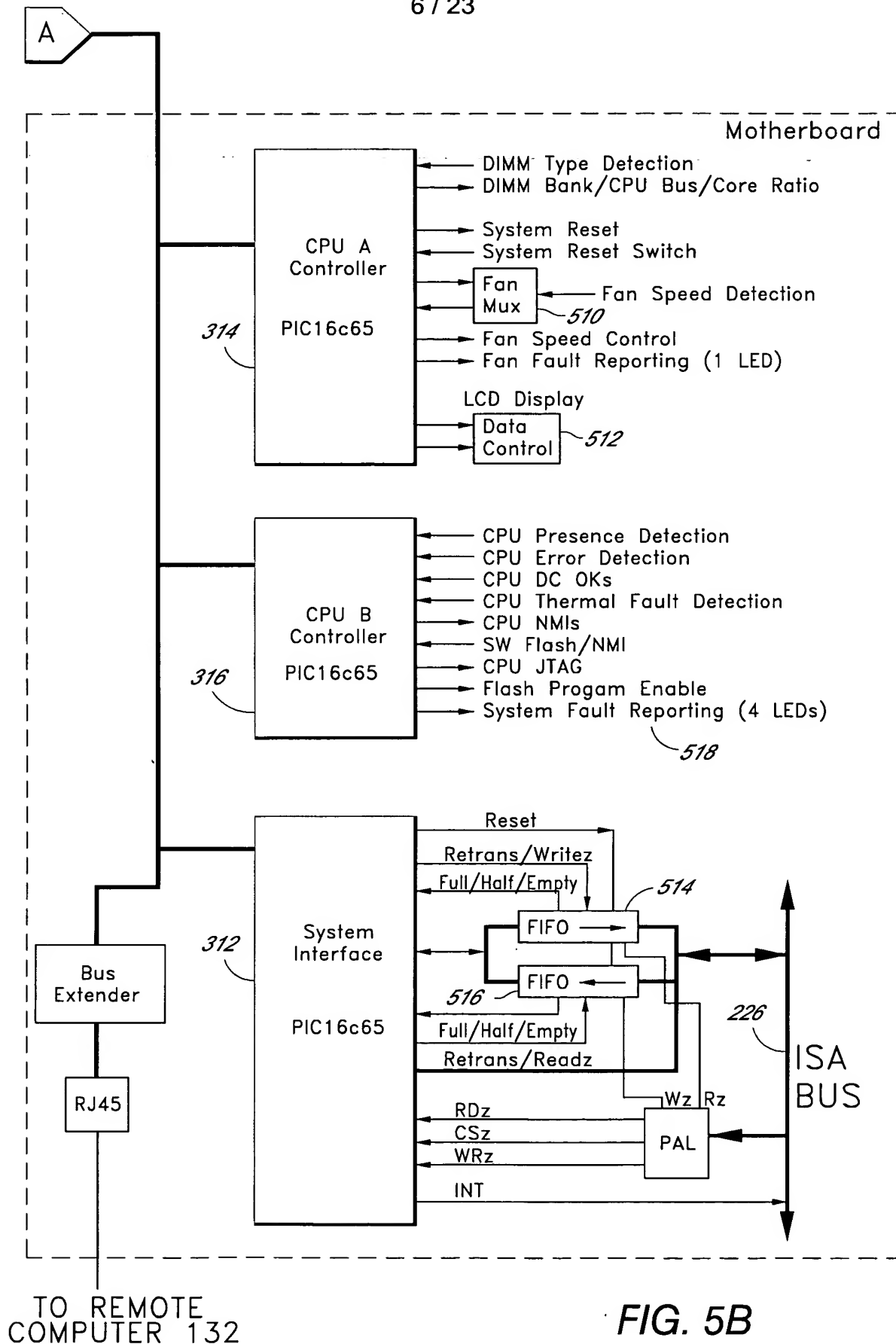


FIG. 5A

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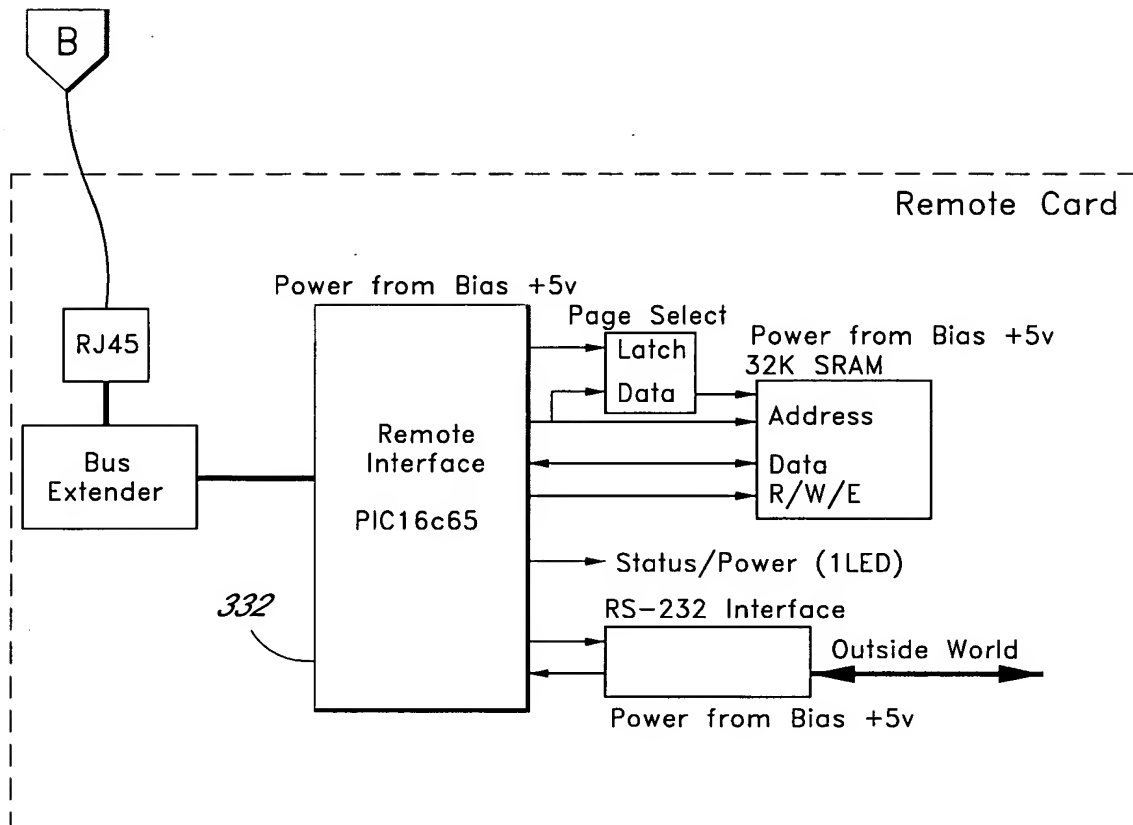


FIG. 5C

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PROCESS FOR REMOTE CONTROL OF LOCAL DIAGNOSTIC SERVICES

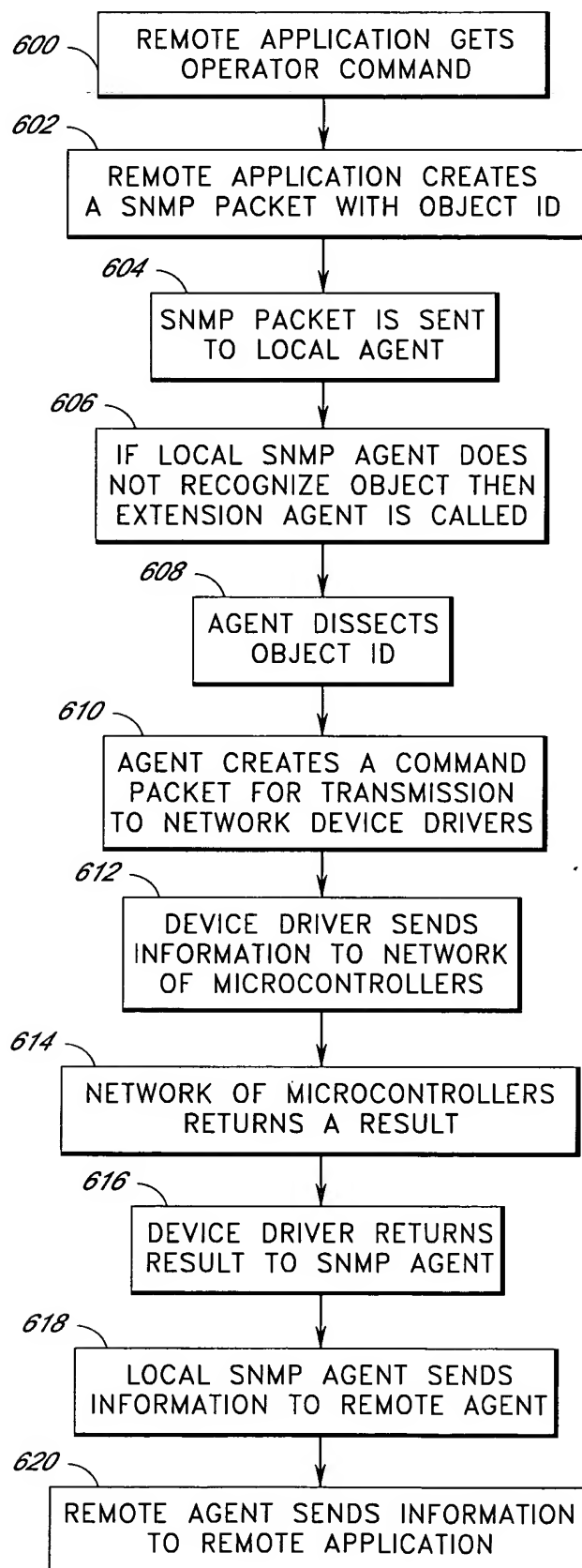


FIG. 6

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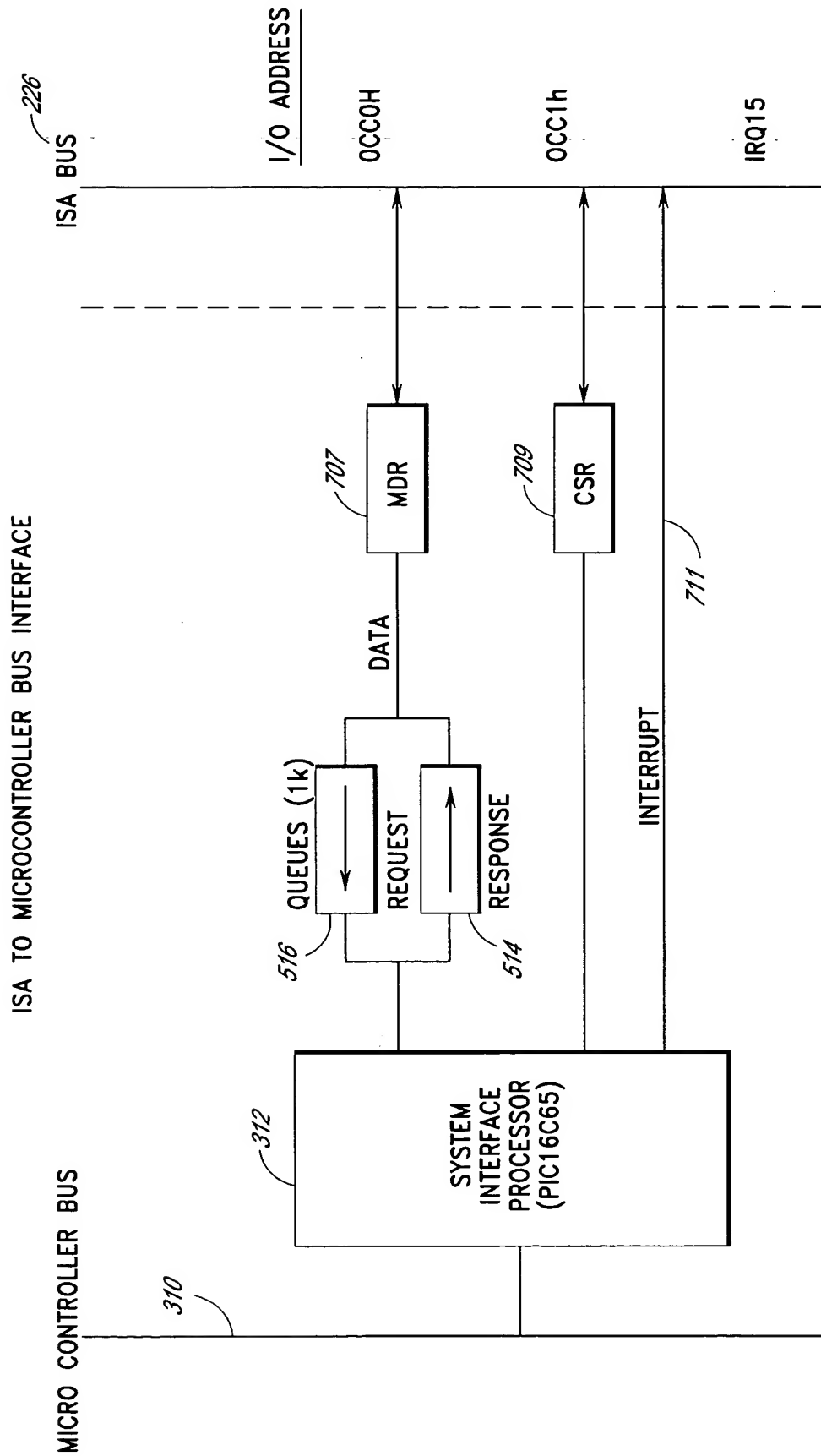


FIG. 7

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MASTER TO SLAVE COMMUNICATION

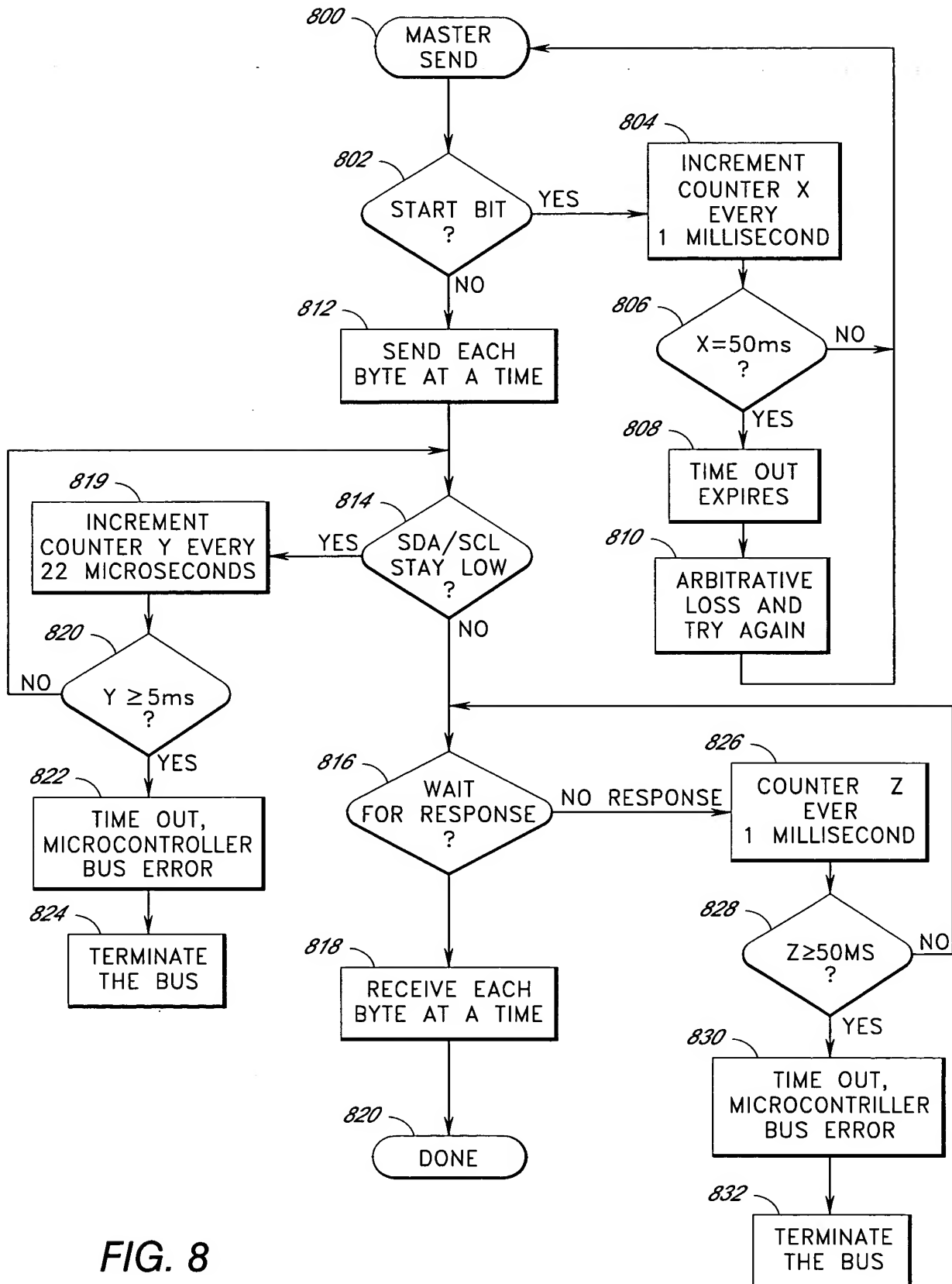


FIG. 8

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SLAVE TO MASTER COMMUNICATION

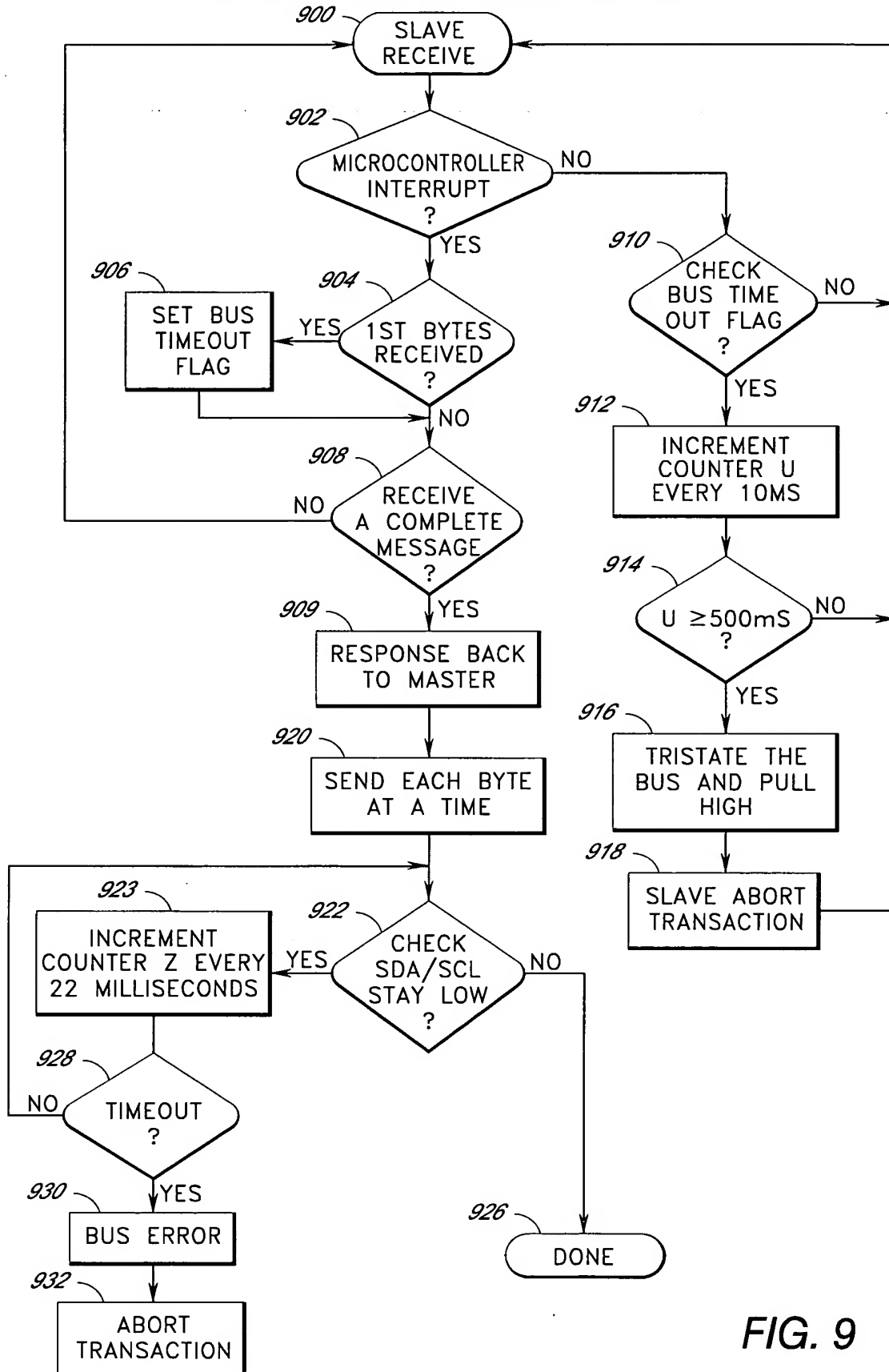
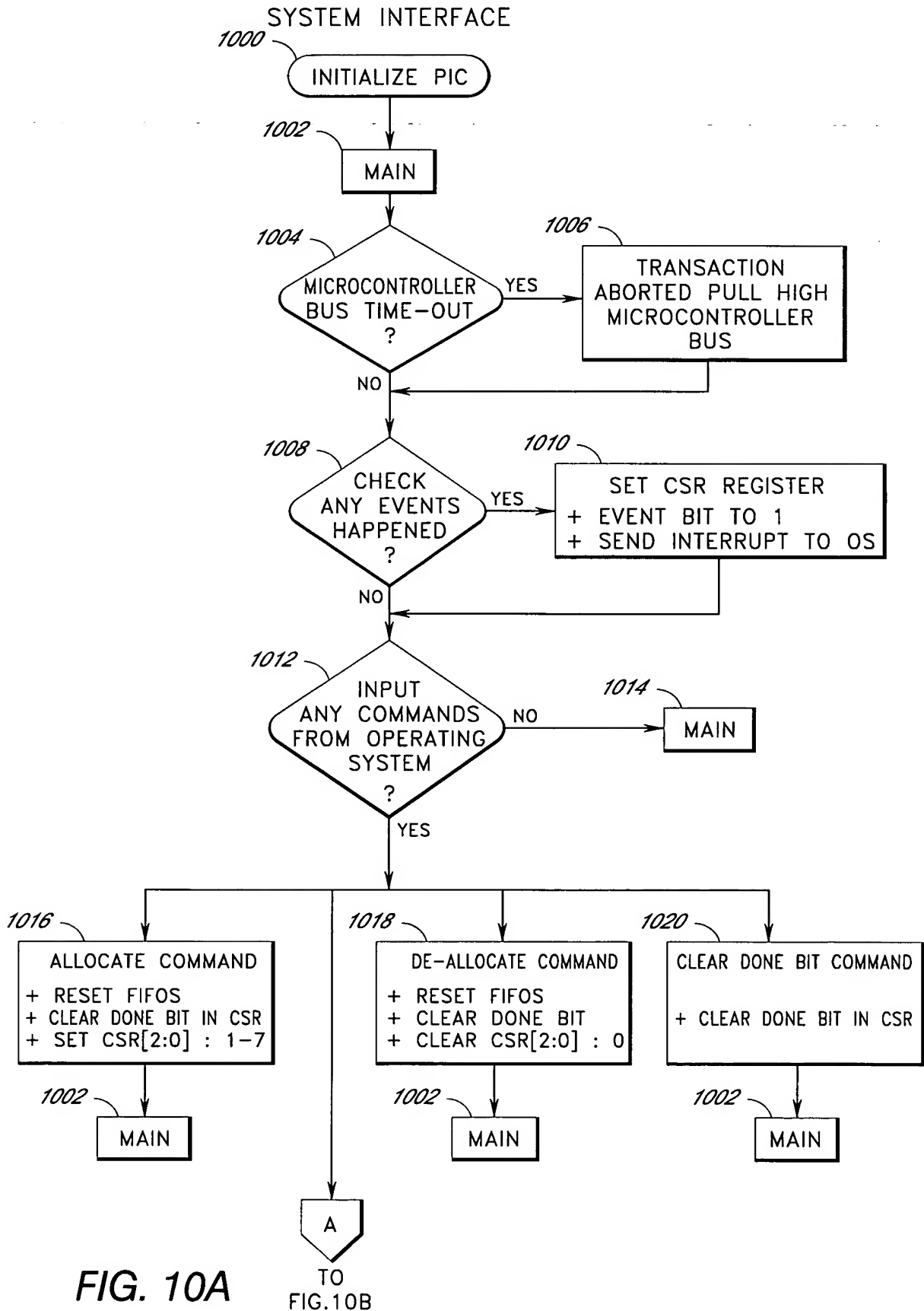


FIG. 9

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SYSTEM INTERFACE (CONTINUED)

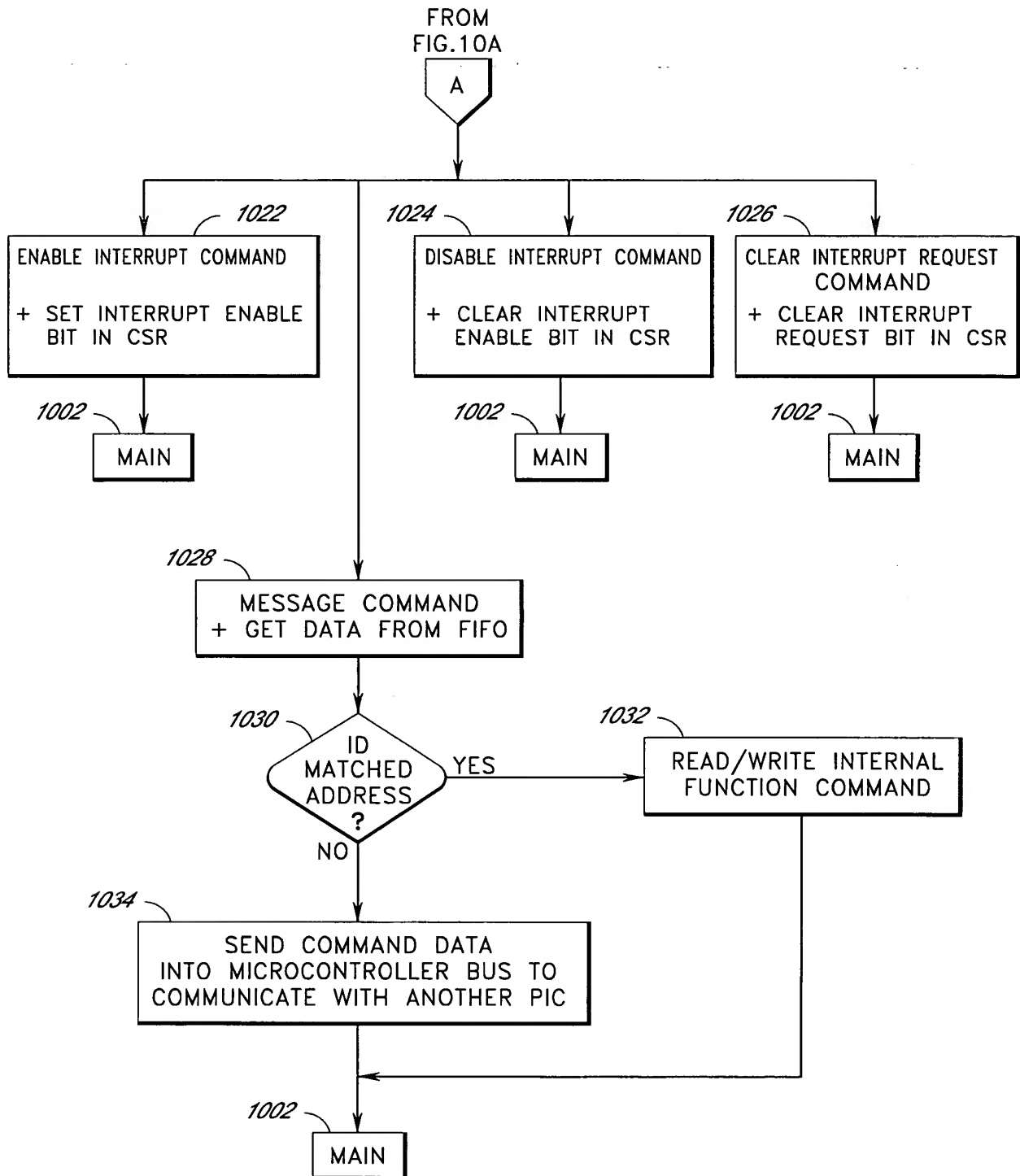


FIG. 10B

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CHASSIS CONTROLLER

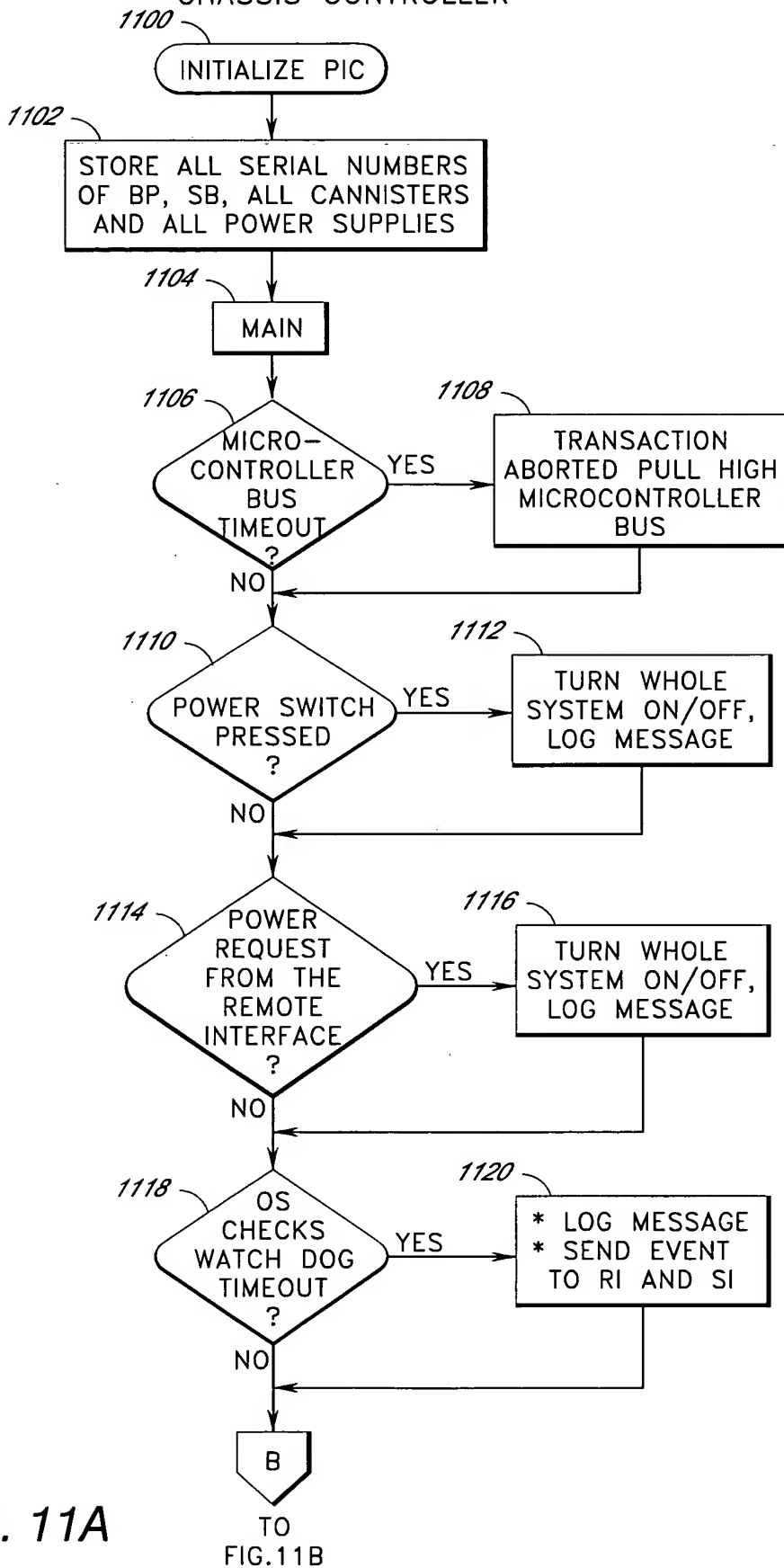


FIG. 11A

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CHASSIS CONTROLLER (CONTINUED)

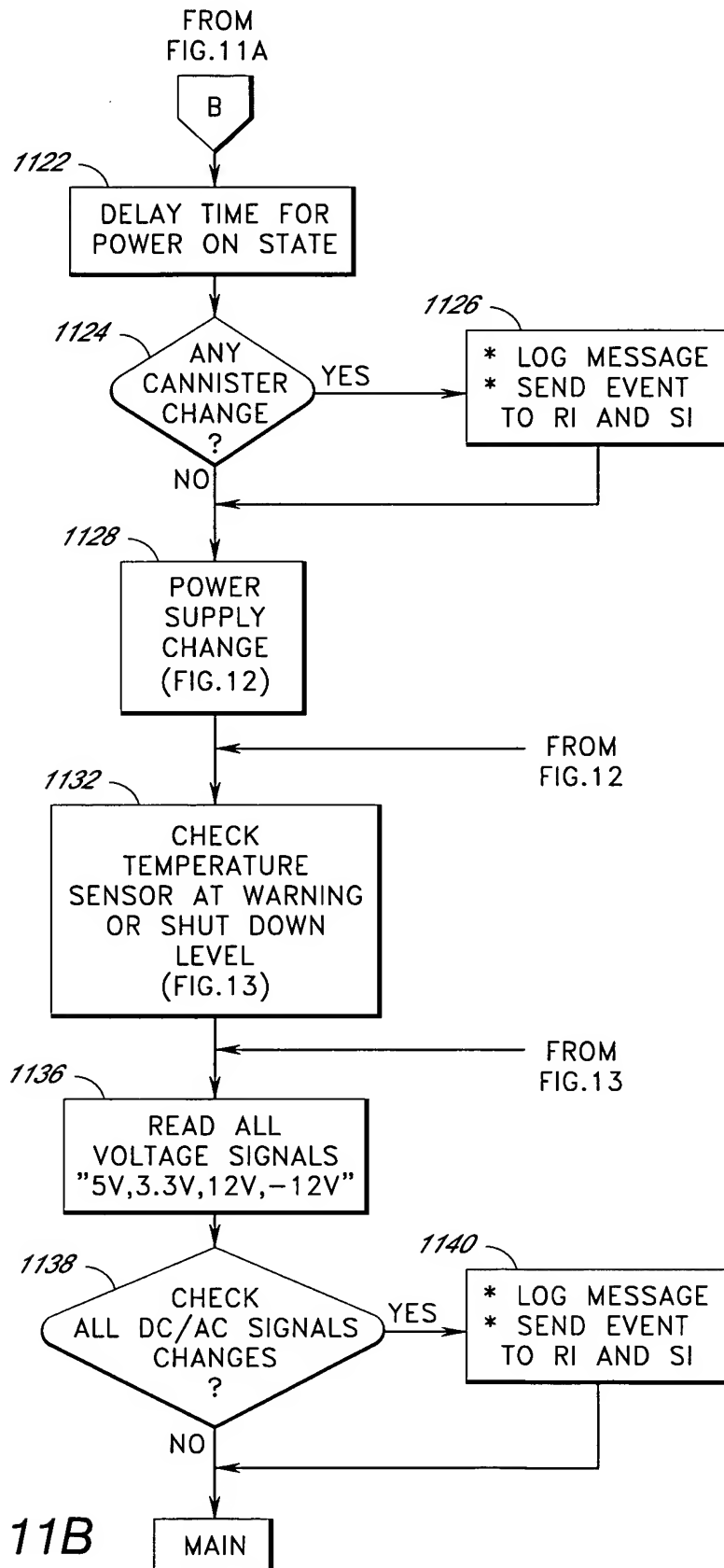


FIG. 11B

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POWER SUPPLY

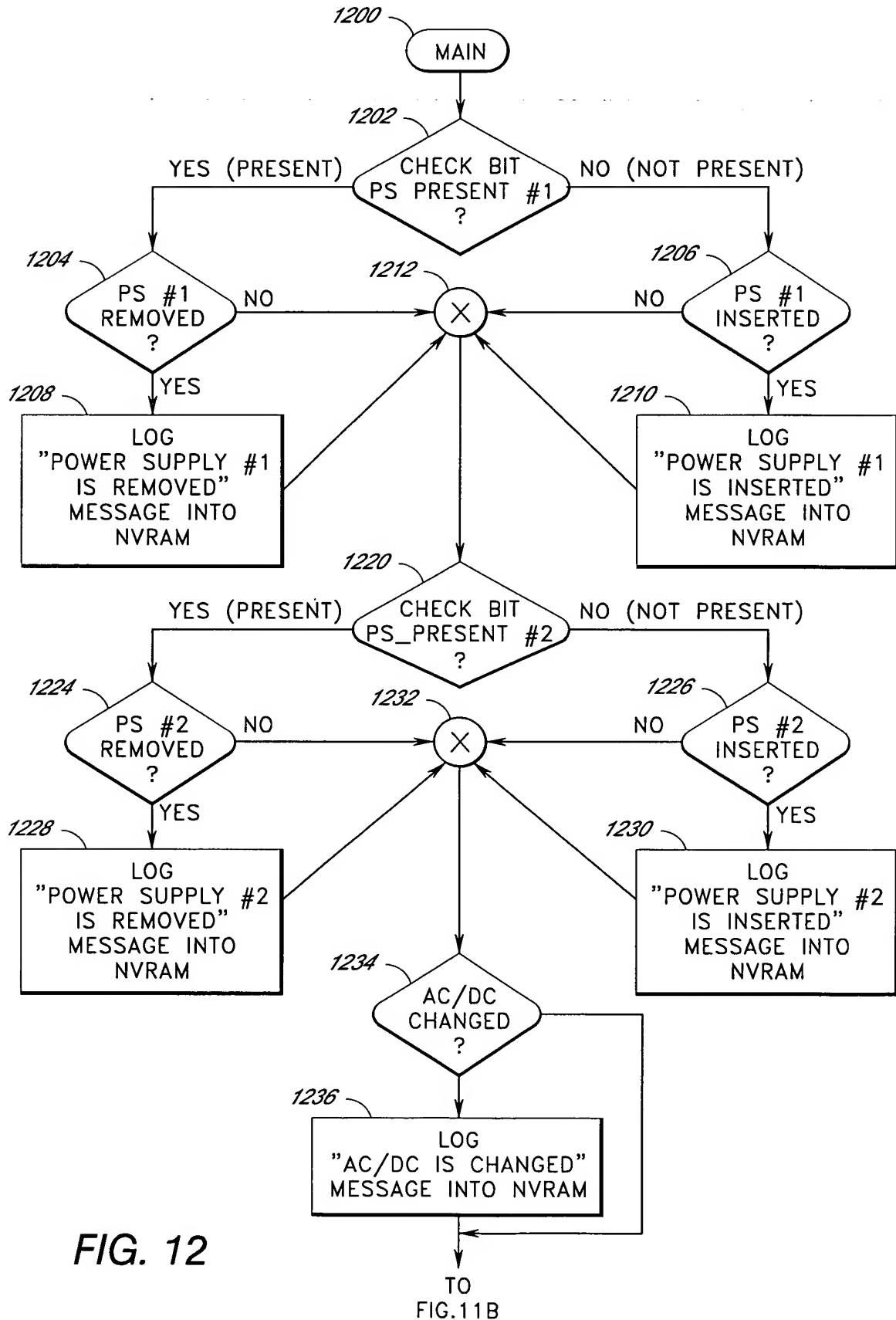


FIG. 12

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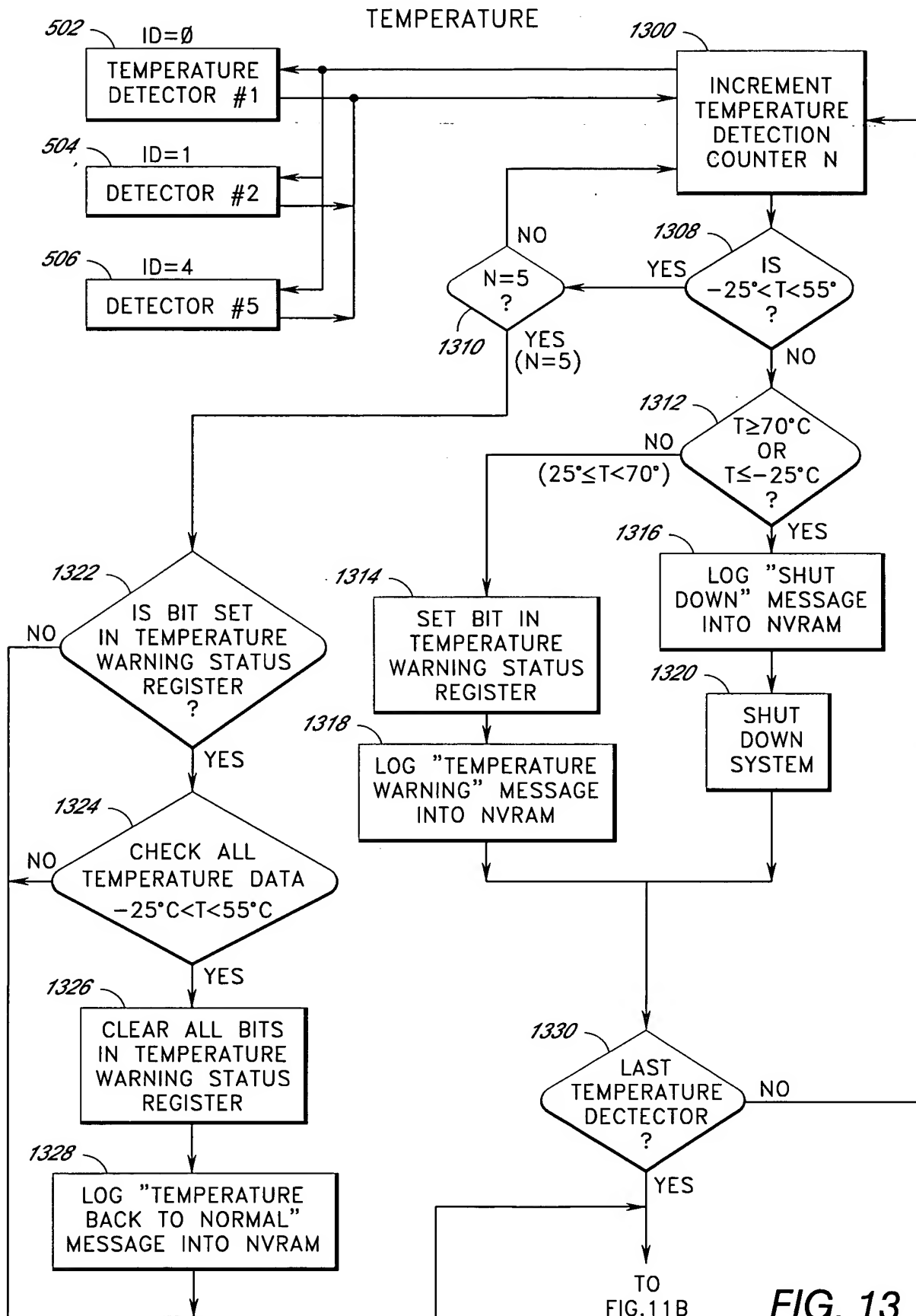


FIG. 13

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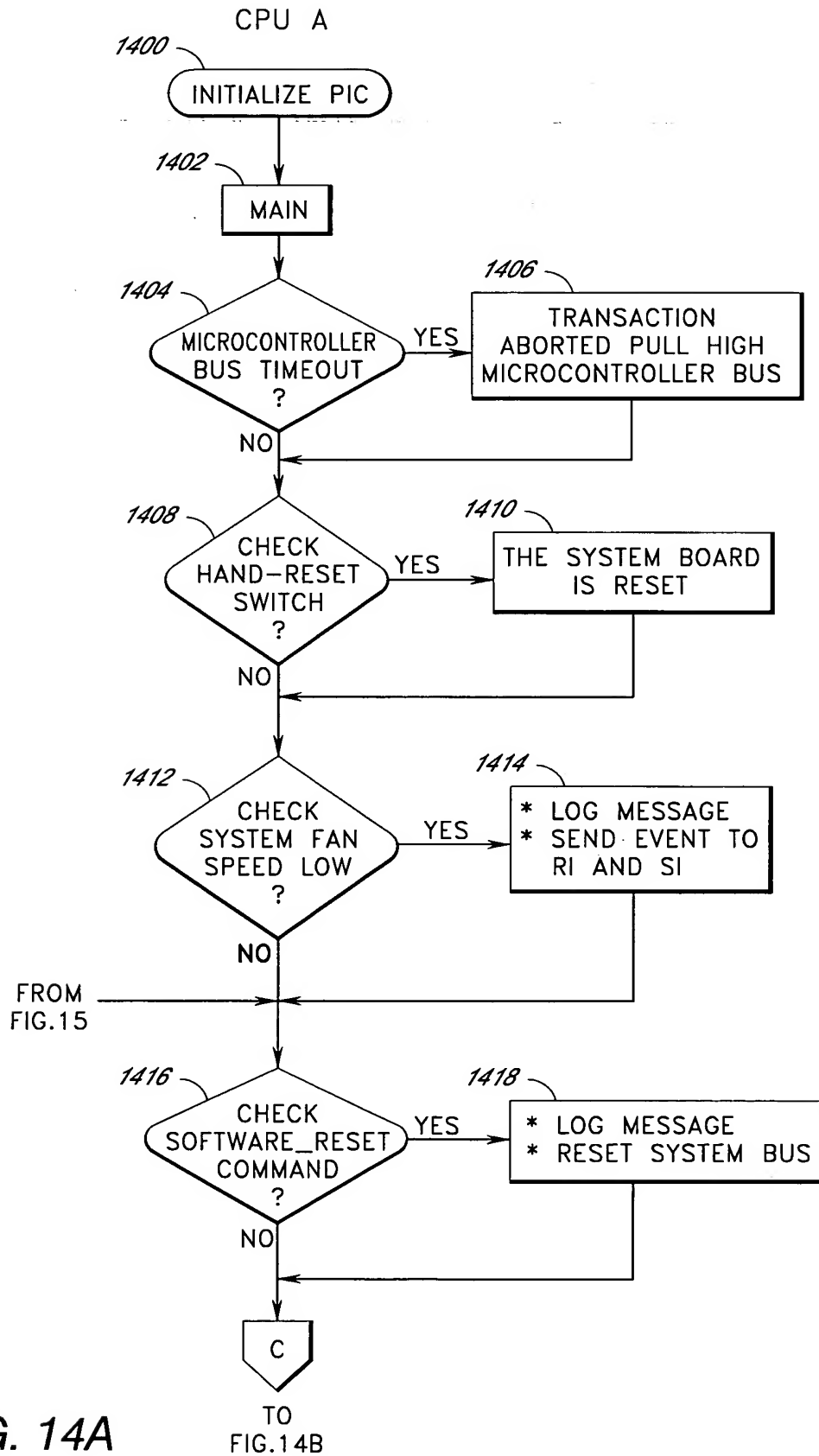


FIG. 14A

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CPU A (CONTINUED)

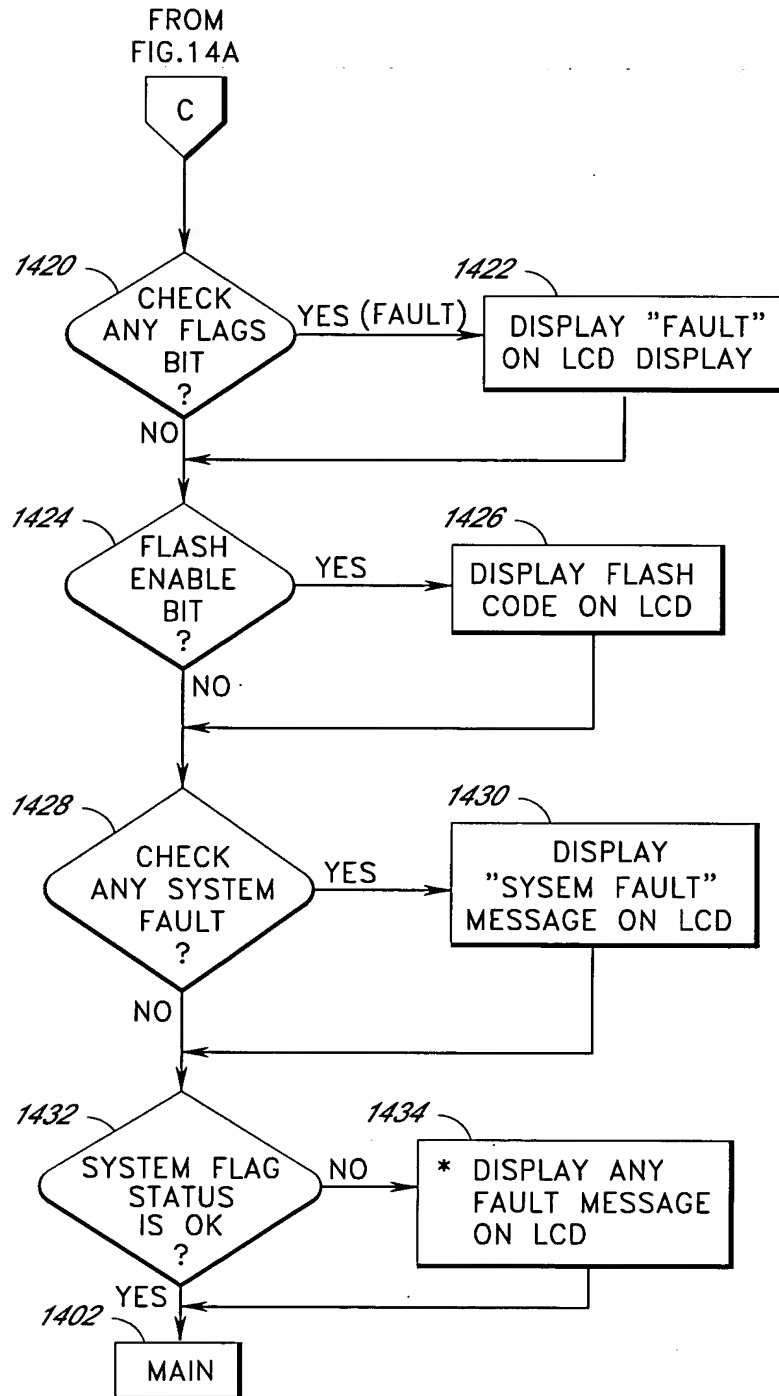


FIG. 14B

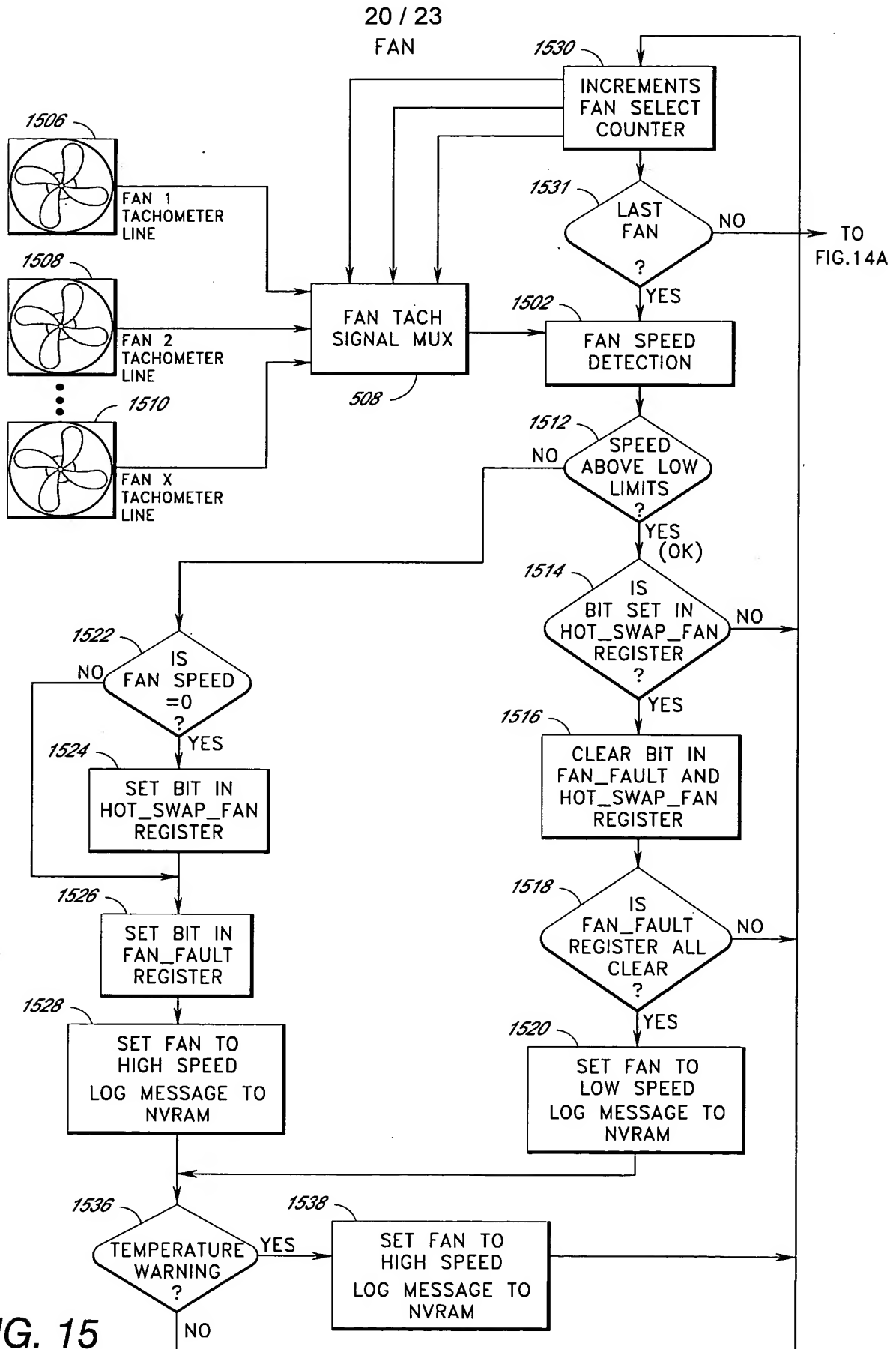


FIG. 15

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CPU B

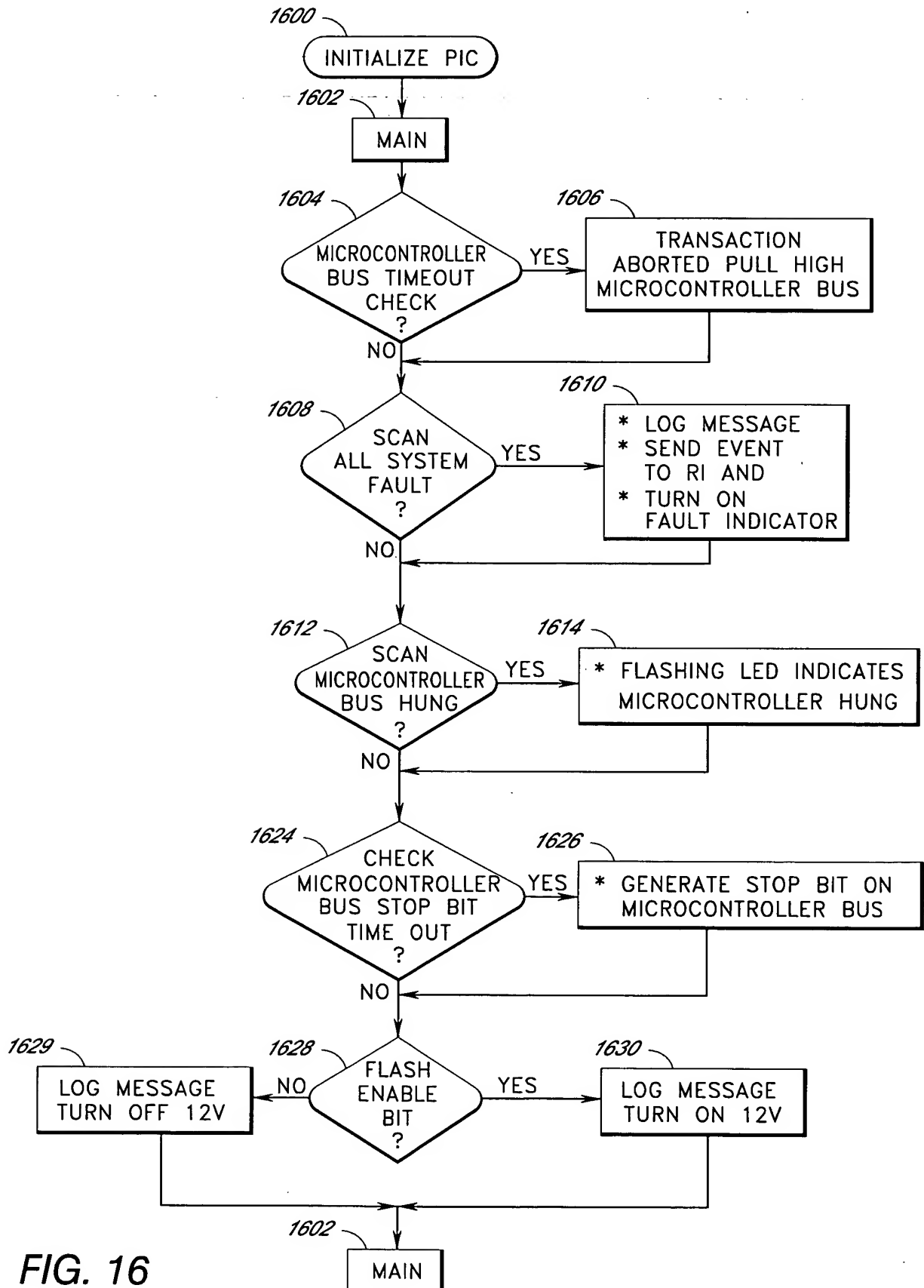


FIG. 16

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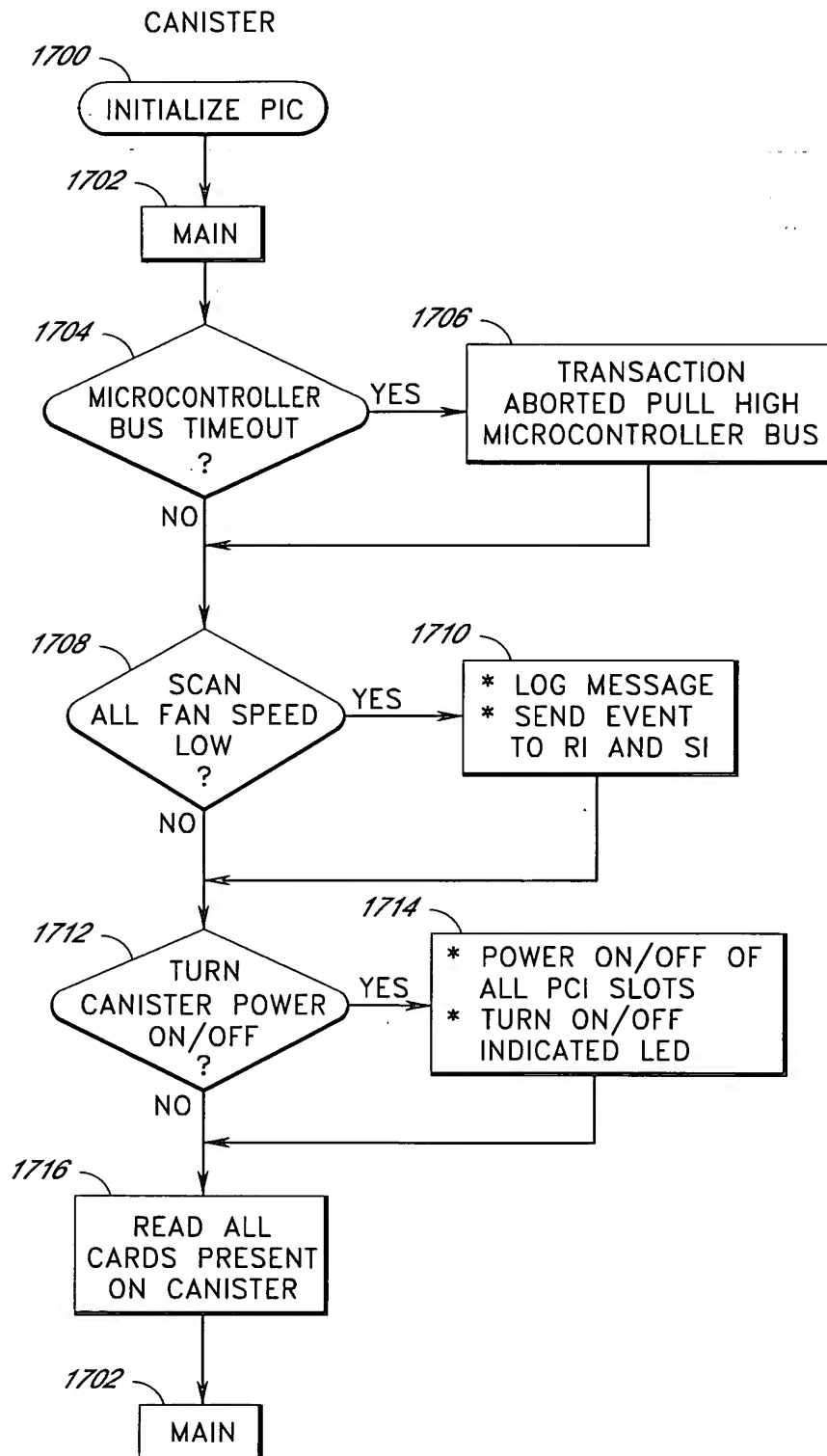


FIG. 17

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SYSTEM RECORDER

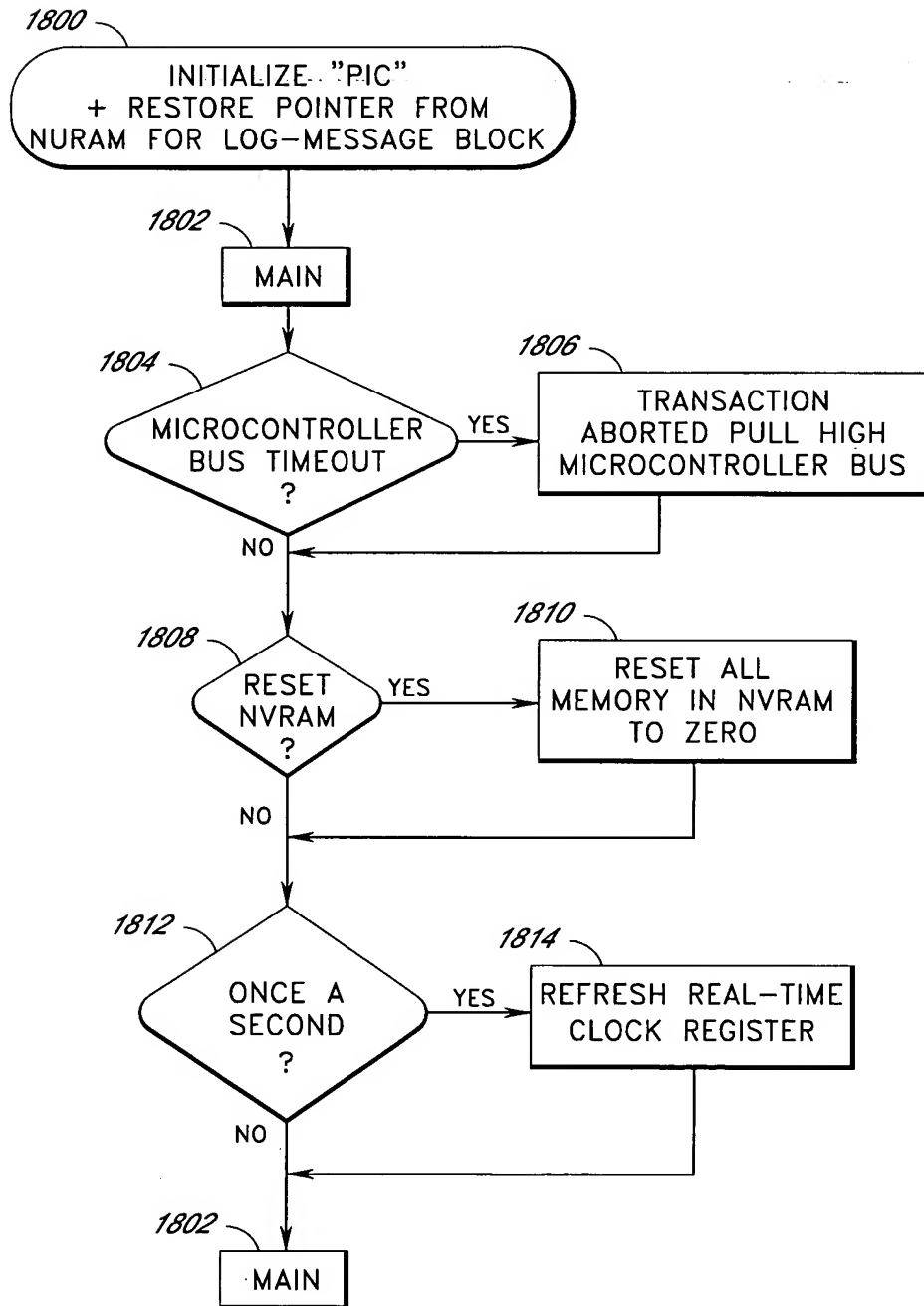


FIG. 18